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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/757,404	01/08/2001	Steven A. Guccione	X-786 US	6382

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XILINX, INC
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EXAMINER

HOGAN, MARY C

ART UNIT	PAPER NUMBER
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2123

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/757,404

Applicant(s)

GUCCIONE ET AL.

Examiner

Mary C Hogan

Art Unit

2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 November 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 January 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

1. This application has been examined.
2. Claims 1-20 have been examined and rejected.

Drawings

3. **Figure 1** should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. For example, **Figure 1** shows two distinct design paths *currently* required for the design of a static circuit implemented in an FPGA which interfaces with a reconfigurable logic coprocessor (**specification paragraph 15**), implying that this is previously known in the art. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Interpretation

4. **Claim 1** fails to specify a step (h). The examiner concludes from examination of the claims and specification that “performing steps (f) – (h)” in step (e) of Claim 1 should read “performing steps (f) – (g)” and further interprets the claims as such.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. **Claims 1-19** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. For example, **Claim 1 part**

(e) states “performing steps (f) – (h)” where no step (h) is disclosed. It is suggested that step (h) should be clearly disclosed in the claims and specification and point to a step in a figure.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. **Claims 1-19** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. **Claim 1, Part (e)** specifies ““performing steps (f) – (h)” where no step (h) is disclosed. The failure to disclose a step (h) renders the claim vague and indefinite.

Allowable Subject Matter

10. **Claims 6-12 and 19** are objected to as being dependent upon a rejected base claim, but would be allowable over the prior art of record if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

12. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. **Claims 1-5, 13-18 and 20** are rejected under 35 U.S.C. 103(a) as being unpatentable over Agrawal et al (U.S. Patent 6,216,257), herein referred to as **Agrawal** and further in view of Williams (U.S. Patent 6,631,508), herein referred to as **Williams**.

14. As to **Claims 1,13 and 20**, **Agrawal** teaches:

- a. reading a configuration bitstream (**column 3, lines 49-55**)
- b. constructing objects in a computer memory, each object corresponding to a configurable element of the PLD as configured in the configuration bitstream and each object having associated therewith an output signal state and one or more input signal states (**column 8, lines 40-44**)

15. As to steps **c-e and Claim 13**, **Agrawal** teaches mapping VHDL constructs to the fine and/or coarse grain resources of the targeted FPGA device/family (**column 9, lines 24-26 and Figure 1A, elements 40 and 41**).

16. **Agrawal** does not expressly disclose the steps involved in mapping VHDL constructs to the fine and/or coarse grain resources of the targeted FPGA device/family.

17. **Williams** teaches an implementation phase in which a circuit design is synthesized into lower-level technology specific representation such as an FPGA netlist. This phase includes mapping the netlist to particular configurable resources of the device (**Column 2, lines 17-22**). The process includes:

- c. generating events in response to signal values in the configuration bitstream, each event including an object identifier (**column 10, line 33-34**) an input signal identifier (**column 10, lines 42-44**), and an input signal state (**column 10 lines 44-45**)

- d. updating the output signal state and an input signal state of a corresponding object in response to the input signal state of the event and type of configurable element (**column 10, lines 47-49**)
 - e. finding the configurable elements that are connected to the output signal if processing an event changes the output signal state of an object (**column 10, lines 52-53**)
18. As to generating events for the objects corresponding to the configurable elements connected to the output signal if processing an event changes the output signal state of an object, it is taught that the design of the circuit is a process that involves simulation and modification (**column 2, lines 22-31**). It is concluded that after modification of the design, the re-mapping of the HDL description to the FPGA specifications after a redesign would involve processing an event that changes the output signal state of an object, and therefore would generate events for the objects corresponding to the configurable elements connected to the output signal.
19. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify mapping VHDL constructs to the fine and/or coarse grain resources of the targeted FPGA device/family as taught in **Agrawal** with the steps as disclosed in **Williams** since the mapping step involves mapping the netlist to particular configurable resources of the device as taught in **Williams** (**column 2, lines 20-22**).
20. As to **Claims 2 and 15**, **Agrawal** teaches the PLD is an FPGA (**column 1, lines 61-67**), further comprising constructing look up table objects corresponding to FPGA lookup tables wherein each lookup table object includes a plurality of input signal attributes and an ordered set of bit values, each bit value addressable by values of the input signal attributes (**column 8, lines 40-44**).
21. As to **Claims 3 and 16**, **Agrawal** teaches each event further including a routing delay value (**column 9, lines 52-58 and Table 1**).

22. As to **Claims 4 and 17**, **Agrawal** teaches adding each event to a last-in-first-out (LIFO) queue and getting each event from the LIFO queue prior to processing the event (**column 3, lines 33-36**). It is concluded that events are the type of elements that would be added to a LIFO queue and that the implementing of these elements involves getting each event from the LIFO queue prior to processing.

23. As to **Claims 5 and 18**, **Agrawal** teaches maintaining a synchronous event LIFO queue for synchronous events and an asynchronous event LIFO queue for asynchronous events (**column 8 line 66-column 9, line 10**). It is taught that “timing constructs” define events that are synchronous or asynchronous and that the LIFO queues discussed above in paragraph 20 could be used to maintain “clock synchronized registers” such as a queue for synchronous events and a queue for asynchronous events.

24. As to **Claim 14**, **Agrawal** teaches simulating the circuit design in response to hardware interface program calls that are selectable for interfacing with a physical device or with a simulation process (**column 14, lines 15-17 and 27-33**).

Conclusion

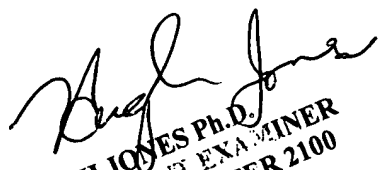
25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mary C Hogan whose telephone number is 703-305-7838. The examiner can normally be reached on 7:30AM-5PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner’s supervisor, Kevin Teska can be reached on 703-305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions

Application/Control Number: 09/757,404
Art Unit: 2123

Page 7

on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197
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